

[Sign in](#)[Web](#) [Images](#) [Groups](#) [News](#) [Froogle](#) [Maps](#) [more »](#)

chips power "TypMax"

Search

[Advanced Search](#)
[Preferences](#)**Web**Results 1 - 8 of about 12 for **chips power "TypMax"**. (0.45 seconds)Did you mean: **chips power "Typ Max"**

Sponsored Links

[PDF] AZ DISPLAYS, INC.File Format: PDF/Adobe Acrobat - [View as HTML](#)**TypMax**. Unit. Operating temperature (Standard) ... **Chip** selection for IC2.H. 17. RST. Reset. L. 18. Vee. **Power** supply for LCD driving ...www.bgmicro.com/pdf/lcd1030.pdf - [Similar pages](#)**Diesel Chips & Tuners**

Superchips, Edge, Diablo, Afe

Duramax, Cummins, Powerstroke

www.pmtdiesel.com**[PDF] IMP52 IMP52 7 7**File Format: PDF/Adobe Acrobat - [View as HTML](#)All four EL lamp-driving functions are on-**chip**. These are the switch- mode **power** supply, its high-frequency oscillator, the high-voltage ...www.impweb.com/IMP527.pdf - [Similar pages](#)**[PDF] Electroluminescent Lamp Drivers**

File Format: PDF/Adobe Acrobat

TypMax. Units. ON-resistance of MOS Switch ... lamp driving functions on-**chip**. These are the switch-mode **power** sup- ply, its high-frequency oscillator, ...www.impweb.com/EL-data-book.pdf - [Similar pages](#)**[PS] SN54HCT32, SN74HCT32QUADRUPLE 2-INPUT POSITIVE-OR GATES SCLS064B ...**File Format: Adobe PostScript - [View as HTML](#)... UNITPARAMETER (INPUT) (OUTPUT) VCC MIN **TYPMAX** MIN MAX MIN MAX UNIT ...PARAMETER TEST CONDITIONS TYP UNIT Cpd **Power** dissipation capacitance per gate

No ...

www.slac.stanford.edu/BFROOT/www/Detector/SVT/Operations/SVTRAD/docs/datasheets/sn74hct32.ps - [Similar pages](#)**[PDF] Description Rule of Property Dictionary**File Format: PDF/Adobe Acrobat - [View as HTML](#)MinMax / MinTyp / **TypMax**. 2-1. To use minimum and maximum ... Apply to rectangular**chip** with terminals or electrode in. opposite direction. Exchangeability ...[ec.jeita.or.jp/home/ecals_ download.cfm?fid=14&lang=en](http://ec.jeita.or.jp/home/ecals_download.cfm?fid=14&lang=en) - [Similar pages](#)**[PDF] プロパティ辞書の記述規約書**File Format: PDF/Adobe Acrobat - [View as HTML](#)2つのレベル識別子で記述可能か？ MinMax / MinTyp / **TypMax**. 2-1. 最小及び最大の 範囲を表現する。 ... Apply to rectangular **chip** with terminals or electrode in ...[ec.jeita.or.jp/home/ecals_ download.cfm?fid=15&lang=ja](http://ec.jeita.or.jp/home/ecals_download.cfm?fid=15&lang=ja) - [Similar pages](#)[[More results from ec.jeita.or.jp](#)]**[PDF] 3 Volt Intel StrataFlash Memory**File Format: PDF/Adobe Acrobat - [View as HTML](#)and system **power** consumption. When configured in level mode (default mode), ... "Chip

Enable Truth Table" on page 16) reduces decoder logic typically ...

[web.mit.edu/6.111/www/s2004/ NEWKIT/datasheets/28F128J3A.pdf](http://web.mit.edu/6.111/www/s2004/NEWKIT/datasheets/28F128J3A.pdf) - [Similar pages](#)**[PDF] Requests for new/update Data Element Types tag meaning obligation ...**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

A reference to a definition of a **power** supply or logic. signal connection ... The total value as specified by level (**typMax**) of the dc ...

tc3.iec.ch/txt/3d014wg.pdf - [Similar pages](#)

In order to show you the most relevant results, we have omitted some entries very similar to the 8 already displayed.

If you like, you can repeat the search with the omitted results included.

Did you mean to search for: chips power "Typ Max"

Info when you want it, right on your desktop
Free! [Download Google Desktop](#)

Google	
News	« ▾
New lines of communication Financial Times 3 hrs ago	
Email	« ▾
Lunch tomorrow? Mandy M Y <.. 11 min ago	
61°F Clear - Mount	« ▾
DJI 10434.87 -84.	« ▾
Type to search	
11:22 AM	

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2006 Google



[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)

Scholar

Results 1 - 1 of 1 for "TypMax". (0.09 seconds)

Did you mean: "[Topmax](#)"

MAXIMUM AND TYPICAL PERFORMANCE

[All articles](#) [Recent articles](#)

E Hoefnagels, RPN Anderson - nsvp.nl

Page 1. MAXIMUM AND TYPICAL PERFORMANCE The effect of Self-Efficacy on Maximum and Typical Performance Esther Hoefnagels University of Amsterdam ...

[View as HTML](#) - [Web Search](#)

Did you mean to search for: "[Topmax](#)"

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2006 Google

Dialog DataStar

[options](#)[logoff](#)[feedback](#)[help](#)[databases](#)[easy
search](#)

Advanced Search:

Inspec - 1898 to date (INZZ)

[limit](#)

Search history:

No.	Database	Search term	Info added since	Results	
1	INZZ	TypMax AND chip AND power	unrestricted	0	-
2	INZZ	TypMax	unrestricted	0	-

[hide](#) | [delete all search steps...](#) | [delete individual search steps...](#)Enter your search term(s): [Search tips](#) ☐ Thesaurus mapping Information added since: or:

(YYYYMMDD)

[search](#)☐ Documents with images

Select special search terms from the following list(s):

- ☒ Publication year 1950-
- ☒ Publication year 1898-1949
- ☒ Inspec thesaurus - browse headings A-G
- ☒ Inspec thesaurus - browse headings H-Q
- ☒ Inspec thesaurus - browse headings R-Z
- ☒ Inspec thesaurus - enter a term
- ☒ Classification codes A: Physics, 0-1
- ☒ Classification codes A: Physics, 2-3
- ☒ Classification codes A: Physics, 4-5
- ☒ Classification codes A: Physics, 6
- ☒ Classification codes A: Physics, 7
- ☒ Classification codes A: Physics, 8
- ☒ Classification codes A: Physics, 9

- ➔ Classification codes B: Electrical & Electronics, 0-5
- ➔ Classification codes B: Electrical & Electronics, 6-9
- ➔ Classification codes C: Computer & Control
- ➔ Classification codes D: Information Technology
- ➔ Classification codes E: Mech., Manufac. & Production Engineering
- ➔ Treatment codes
- ➔ Inspec sub-file
- ➔ Language of publication
- ➔ Publication types

Top - News & FAQs - Dialog

© **2006** Dialog


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide

THE ACM DIGITAL LIBRARY


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

 Terms used TypMax power and chip

Found 9,693 of 177,263

Sort results by

☒ [Save results to a Binder](#)
[Try an Advanced Search](#)

Display results

☐ [Search Tips](#)
[Try this search in The ACM Guide](#)
☐ Open results in a new window

Results 1 - 20 of 200

 Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

 Relevance scale ☐ ☐ ☐ ☐ ☐

1 [Circuit design and modeling: Maximum effective distance of on-chip decoupling](#)



[capacitors in power distribution grids](#)

 Mikhail Popovich, Eby G. Friedman, Michael Sotman, Avinoam Kolodny, Radu M. Secareanu
 April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**

Publisher: ACM Press

 Full text available: [pdf\(524.44 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Decoupling capacitors are widely used to reduce power supply noise. On-chip decoupling capacitors have traditionally been allocated into the available white space on a die. The efficacy of on-chip decoupling capacitors depends upon the impedance of the power/ground lines connecting the capacitors to the current loads and power supplies. A maximum effective radius exists for each on-chip decoupling capacitor. Beyond this effective distance, a decoupling capacitor is completely ineffective. Two ef ...

Keywords: decoupling capacitors, power distribution grids, power distribution systems

2 [Power, buffering and open source: Effects of on-chip inductance on power](#)



[distribution grid](#)

 Atsushi Muramatsu, Masanori Hashimoto, Hidetoshi Onodera
 April 2005 **Proceedings of the 2005 international symposium on Physical design ISPD '05**

Publisher: ACM Press

 Full text available: [pdf\(362.07 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

With increase of clock frequency, on-chip wire inductance starts to play an important role in power/ground distribution analysis, although it has not been considered so far. We perform a case study work that evaluates relation between decoupling capacitance position and noise suppression effect, and we reveal that placing decoupling capacitance close to current load is necessary for noise reduction. We experimentally show that impact of on-chip inductance becomes small when on-chip decoupling ca ...

Keywords: decoupling capacitance, on-chip inductance, power distribution network, power supply noise

3 [Power supply noise analysis methodology for deep-submicron VLSI chip design](#)



Howard H. Chen, David D. Ling



June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**

Publisher: ACM Press

Full text available: [pdf\(237.07 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)



[Publisher Site](#)

This paper describes a new design methodology to analyze the on-chip power supply noise for high-performance microprocessors. Based on an integrated package-level and chip-level power bus model, and a simulated switching circuit model for each functional block, this methodology offers the most complete and accurate analysis of Vdd distribution for the entire chip. The analysis results not only provide designers with the inductive ΔI noise and the resistive IR drop data at the same time, but also allow d ...

4 Power-driven Design of Router Microarchitectures in On-chip Networks

Hangsheng Wang, Li-Shiuan Peh, Sharad Malik

December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: [pdf\(255.15 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

As demand for bandwidth increases in systems-on-a-chip and chip multiprocessors, networks are fast replacing buses and dedicated wires as the pervasive interconnect fabric for on-chip communication. The tight delay requirements faced by on-chip networks have resulted in prior microarchitectures being largely performance-driven. While performance is a critical metric, on-chip networks are also extremely power-constrained. In this paper, we investigate on-chip network microarchitectures from a power-drive ...

5 Energy aware design: Power protocol: reducing power dissipation on off-chip data buses

K. Basu, A. Choudhary, J. Pisharath, M. Kandemir

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society Press

Full text available: [pdf\(1.18 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

[Publisher Site](#)

Power consumption is becoming increasingly important for both embedded and high-performance systems. Off-chip data buses can be a major power consumer. In this paper, we present a strategy called "power protocol" that tries to reduce the dynamic power dissipation on off-chip data buses. To accomplish this, our strategy reduces the number of bus lines that need to be activated for data transfer by employing a small cache (called "value cache") at each side of the off-chip data bus. These value cac ...

6 Low power memory system: System level power-performance trade-offs in embedded systems using voltage and frequency scaling of off-chip buses and memory



Kiran Puttaswamy, Kyu-Won Choi, Jun Cheol Park, Vincent J. Mooney, Abhijit Chatterjee, Peeter Ellervee

October 2002 **Proceedings of the 15th international symposium on System Synthesis**

Publisher: ACM Press

Full text available: [pdf\(84.16 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In embedded systems, off-chip buses and memory (i.e., L2 memory as opposed to the L1 memory which is usually on-chip cache) consume significant power, often more than the processor itself. In this paper, for the case of an embedded system with one processor chip and one memory chip, we propose frequency and voltage scaling of the off-chip

buses and the memory chip and use a known micro-architectural enhancement called a store buffer to reduce the resulting impact on execution time. Our benchmark ...

Keywords: design space, embedded systems, power-performance trade-offs, voltage/frequency scaling

7 Power Grid and Signal Integrity Analysis: Scaling trends of on-chip Power distribution noise



Andrey V. Mezhiba, Eby G. Friedman

April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**

Publisher: ACM Press

Full text available: pdf(110.79 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The design of power distribution networks in high performance integrated circuits has become significantly more challenging with recent advances in process technology. As on-chip currents exceed tens of amperes and circuit clock periods are reduced well below a nanosecond, the signal integrity of the on-chip power supply has become a primary concern in integrated circuit design. The existing work on power distribution noise scaling is reviewed and extended to include the scaling of the inductanc ...

Keywords: power distribution, power supply noise, technology scaling

8 System design methodology: Replacing global wires with an on-chip network: a power analysis



Seongmoo Heo, Krste Asanović

August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**

Publisher: ACM Press

Full text available: pdf(250.91 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper explores the power implications of replacing global chip wires with an on-chip network. We optimize network links by varying repeater spacing, link pipelining, and voltage scaling, to significantly reduce the energy to send a bit across chip. We develop an analytic model of large chip designs with an on-chip two-dimensional mesh network and estimate the power savings possible in a 70 nm process for two different design points: a circuit-switched ASIC or FPGA design, and a dynamic pack ...

Keywords: on-chip network power model, pipelining, router, tile size, tiled architecture, wire power model

9 Leakage estimation: Full chip leakage estimation considering power supply and temperature variations



Haihua Su, Frank Liu, Anirudh Devgan, Emrah Acar, Sani Nassif

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(1.15 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Leakage power is emerging as a key design challenge in current and future CMOS designs. Since leakage is critically dependent on operating temperature and power supply, we present a full chip leakage estimation technique which accurately accounts for power

supply and temperature variations. State of the art techniques are used to compute the thermal and power supply profile of the entire chip. Closed-form models are presented which relate leakage to temperature and VDD variations. These models c ...

Keywords: leakage power, supply voltage variation, thermal analysis

10 Managing power and performance for System-on-Chip designs using Voltage Islands



David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

Full text available:  [pdf\(96.51 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption. Effectiv ...


11 Low power SOC's and NOCs: High-level power analysis for on-chip networks



Noel Easley, Li-Shiuan Peh

September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems**

Publisher: ACM Press

Full text available:  [pdf\(353.56 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

As on-chip networks become prevalent in multiprocessor systems-on-a-chip and multi-core processors, they will be an integral part of the design flow of such systems. With power increasingly the primary constraint in chips, the tool chain in systems design, from simulation infrastructures to compilers and synthesis frameworks, needs to take network power into account, motivating the need for early-stage communication power analysis. While there has been substantial research in network performance ...

Keywords: link utilization, power analysis, simulation, systems-on-a-chip (SoC)


12 Poster Session 1: FIFO power optimization for on-chip networks



Sudarshan Banerjee, Nikil Dutt

April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Publisher: ACM Press

Full text available:  [pdf\(105.29 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

As the design community moves towards architecting multiprocessor systems-on-chip (MPSoC), it is widely believed that an on-chip interconnection network is potentially the best candidate to satisfy the high aggregate throughput needed by dozens of IP blocks. In this context, power (energy) estimation and reduction techniques for switches and links, the core components of an interconnection network, gain added significance. FIFO buffers are a key component of a majority of network switches - buff ...

Keywords: FIFO, low power design, on-chip networks, shared memory, switches, wide flits

13 An experimental system for power/timing optimization of LSI chips

B. J. Agule, J. D. Lesser, A. E. Ruehli, P. K. Wolff

January 1977 **Proceedings of the 14th conference on Design automation****Publisher:** IEEE PressFull text available:  [pdf\(423.02 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

An experimental system of programs is described which places logic gates on a chip, globally wires the gates and then optimizes the power required to drive them. Further power reductions are realized by using power-oriented placement improvement techniques. A companion paper describes how the optimization is accomplished by using the timing requirements of the chip as constraints and assigning delays to the logic gates so that these constraints are met and the power is minimized.

14 Power distribution issues: Macro-modeling concepts for the chip electrical interface Brian W. Amick, Claude R. Gauthier, Dean LiuJune 2002 **Proceedings of the 39th conference on Design automation****Publisher:** ACM PressFull text available:  [pdf\(515.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The power delivery network is made up of passive elements in the distribution network, as well as the active transistor loads. A chip typically has three types of power supplies that require attention: core, I/O, and analog. Core circuits consist of digital circuits and have the largest current demand. In addition to all of the system issues/models for the core, modeling the I/O subsystem has the additional requirement of modeling return paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor design, inductance

15 Clock, power grid and thermal analysis and optimization: Fast computation of the temperature distribution in VLSI chips using the discrete cosine transform and table look-up Yong Zhan, Sachin S. SapatnekarJanuary 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05****Publisher:** ACM PressFull text available:  [pdf\(1.25 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#)

Temperature-related effects are critical in determining both the performance and reliability of VLSI circuits. Accurate and efficient estimation of the temperature distribution corresponding to a specific circuit layout is indispensable in physical design automation tools. In this paper, we propose a highly accurate fast algorithm for computing the on-chip temperature distribution due to power sources located on the top surface of the chip. The method is a combination of several computational te ...

16 Power-performance considerations of parallel computing on chip multiprocessors Jian Li, José F. MartínezDecember 2005 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 2 Issue 4**Publisher:** ACM PressFull text available:  [pdf\(565.90 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper looks at the power-performance implications of running parallel applications on chip multiprocessors (CMPs). First, we develop an analytical model that, for the first time, puts together parallel efficiency, granularity of parallelism, and voltage/frequency scaling,

to establish a formal connection with the power consumption and performance of a parallel code running on a CMP. We then conduct detailed simulations of parallel applications running on a detailed power-performance CMP mod ...

Keywords: Voltage/frequency scaling, granularity, parallel efficiency

17 Compiler-directed channel allocation for saving power in on-chip networks



Guangyu Chen, Feihui Li, Mahmut Kandemir

January 2006 **ACM SIGPLAN Notices , Conference record of the 33rd ACM SIGPLAN-SIGACT symposium on Principles of programming languages POPL '06**, Volume 41 Issue 1

Publisher: ACM Press

Full text available: pdf(943.11 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Increasing complexity in the communication patterns of embedded applications parallelized over multiple processing units makes it difficult to continue using the traditional bus-based on-chip communication techniques. The main contribution of this paper is to demonstrate the importance of compiler technology in reducing power consumption of applications designed for emerging multi processor, NoC (Network-on-Chip) based embedded systems. Specifically, we propose and evaluate a compiler-directed a ...

Keywords: NoC, compiler, energy consumption

18 Power grid, thermal, and leakage issues: The need for a full-chip and package



thermal model for thermally optimized IC designs

Wei Huang, Eric Humenay, Kevin Skadron, Mircea R. Stan

August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**

Publisher: ACM Press

Full text available: pdf(1.08 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Modeling and analyzing detailed die temperature with a full-chip thermal model at early design stages is important to discover and avoid potential thermal hazards. However, omitting important aspects of *package* details in a thermal model can result in significant temperature estimation errors. In this paper, we discuss the applications of an existing compact thermal model that models both *die* and *package* temperature details. As an example, a thermally self-consistent leakage ...

Keywords: leakage, package, temperature-aware design, thermal model

19 Model and analysis for combined package and on-chip power grid simulation



Rajendran Panda, David Blaauw, Rajat Chaudhry, Vladimir Zolotov, Brian Young, Ravi Ramaraju

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(220.58 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present new modeling and simulation techniques to improve the accuracy and efficiency of transient analysis of large power distribution grids. These include an accurate model for the inherent decoupling capacitance of non-switching devices, as well as a statistical switching current model for the switching devices. Moreover, three new simulation techniques are presented for problem size-reduction and speed-up. Results of

application of these techniques on three PowerPCtm

20 On-chip communication architectures: analysis and optimisation: Power analysis of system-level on-chip communication architectures



Kanishka Lahiri, Anand Raghunathan

September 2004 **Proceedings of the 2nd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Publisher: ACM Press

Full text available:  pdf(101.16 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

For complex System-on-chips (SoCs) fabricated in nanometer technologies, the system-level on-chip communication architecture is emerging as a significant source of power consumption. Managing and optimizing this important component of SoC power requires a detailed understanding of the characteristics of its power consumption. Various power estimation and low-power design techniques have been proposed for the global interconnects that form part of SoC communication architectures (e.g., low- ...

Keywords: communication architectures, low-power design, network-on-chip, power analysis, system-on-chip

Results 1 - 20 of 200

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2006 ACM, Inc.

[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

Useful downloads:  [Adobe Acrobat](#)  [QuickTime](#)  [Windows Media Player](#)  [Real Player](#)

[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)Search: ☒ The ACM Digital Library ☐ The Guide

Nothing Found

Your search for "**TypMax**" did not return any results.

You may want to try an [Advanced Search](#) for additional options.

Please review the [Quick Tips](#) below or for more information see the [Search Tips](#).

Quick Tips

- Enter your search terms in lower case with a space between the terms.

sales offices

You can also enter a full question or concept in plain language.

Where are the sales offices?

- Capitalize proper nouns to search for specific people, places, or products.

John Colter, Netscape Navigator

- Enclose a phrase in double quotes to search for that exact phrase.

"museum of natural history" "museum of modern art"

- Narrow your searches by using a + if a search term must appear on a page.

museum +art

- Exclude pages by using a - if a search term must not appear on a page.

museum -Paris

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

museum +"natural history" dinosaur -Chicago

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2006 ACM, Inc.

[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

Useful downloads:  [Adobe Acrobat](#)  [QuickTime](#)  [Windows Media Player](#)  [Real Player](#)

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((typmax)<and> chip)<in>metadata)"

☒ e-mail

Your search matched 0 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.

» Search Options

[View Session History](#)[New Search](#)

Modify Search

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance search.

[Help](#) [Contact Us](#) [Privacy & :>](#)

© Copyright 2006 IEEE –

Indexed by
 Inspect

[Sign in](#)[Web](#) [Images](#) [Groups](#) [News](#) [Froogle](#) [Maps](#) [more »](#)

MAX MIN TypMax "chip" -2006 -2005 -2004 -2003 -2002 -2001

[Advanced Search](#)
[Preferences](#)**Web** Results 1 - 3 of 3 for **MAX MIN TypMax "chip" -2006 -2005 -2004 -2003 -2002 -2001**. (0.30 seconds)Did you mean: **MAX MIN Typ Max "chip" -2006 -2005 -2004 -2003 -2002 -2001**[\[PS\] SN54HCT32, SN74HCT32QUADRUPLE 2-INPUT POSITIVE-OR GATES SCLS064B ...](#)File Format: Adobe PostScript - [View as HTML](#)

SN54HCT32 SN74HCT32 UNIT MIN NOM MAX MINNOM MAX UNIT VCC Supply voltage

4.5 5 5.5 4.5 ... UNITPARAMETER (INPUT) (OUTPUT) VCC MIN TYPMAX MIN MAX MIN

MAX UNIT ...

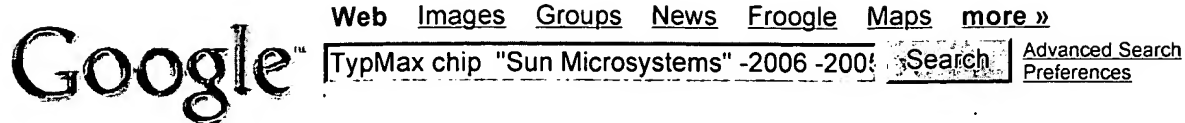
www.slac.stanford.edu/BFROOT/www/Detector/SVT/Operations/SVTRAD/docs/datasheets/sn74hct32.ps - [Similar pages](#)[\[PDF\] TYPES SN7402, SN74LS02, SN74S02 SN5402, SN54LS02, SN54S02 ...](#)File Format: PDF/Adobe Acrobat - [View as HTML](#)Ceramic **Chip** Carrier (FK) Package. SN5402, SN54LS02, SN54S02 ... J PACKAGE ...shown SI **MIN** Or **MAX** . use the appropriate value r pacifi*d under rwommendad ...[www.produktinfo.conrad.com/datenblaetter/150000-174999/170038-da-01-en-](http://www.produktinfo.conrad.com/datenblaetter/150000-174999/170038-da-01-en-sn_7402_n_5402_74ls02_54ls02.pdf)sn_7402_n_5402_74ls02_54ls02.pdf - [Similar pages](#)[\[PDF\] Requests for new/update Data Element Types tag meaning obligation ...](#)File Format: PDF/Adobe Acrobat - [View as HTML](#)AAE072: Definition modified (minmax -. -> **max**). DET for **min** value added. separate (X1-29). ... The total value as specified by level (**typMax**) of the dc ...tc3.iec.ch/txt/3d014wg.pdf - [Similar pages](#)Did you mean to search for: **MAX MIN Typ Max "chip" -2006 -2005 -2004 -2003 -2002 -2001**Free! Speed up the web. [Download the Google Web Accelerator.](#)

MAX MIN TypMax "chip" -2006 -2005 -2004 -2003 -2002 -2001

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2006 Google

[Sign in](#)



Web

Tip: Try removing quotes from your search to get more results.

Your search - **TypMax chip "Sun Microsystems" -2006 -2005 -2004 -2003 -2002 -2001** - did not match any documents.

Suggestions:

- Make sure all words are spelled correctly.
- Try different keywords.
- Try more general keywords.
- Try fewer keywords.

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2006 Google

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	9	(multi adj cycle) same derivative	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 14:30
2	BRS	L2	1	(multi adj cycle adj derivative)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 14:34
3	BRS	L3	2	(TypMax)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 14:35
4	BRS	L4	186	703/18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 14:59
5	BRS	L5	1	(single adj cycle adj summary)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:00

	Comments	Error Definition	Errors
1			
2			
3			
4			
5			

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	0	(multi-cycle adj summary)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:02
7	BRS	L7	383	716/4.ccls. and (power same value\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:02
8	BRS	L9	1	716/4.ccls. and (power same value\$2) and (cycles same plurality) and derivative	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:03
9	BRS	L8	19	716/4.ccls. and (power same value\$2) and (cycles same plurality)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:03
10	BRS	L10	11	716/4.ccls. and (power same value\$2) and (cycles same plurality) and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:03

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	11	716/4.ccls. and (power same value\$2) and (cycles same plurality) and (chip same power)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/04 15:05
12	BRS	L12	0	716/4.ccls. and (power same min same max) and (cycles same plurality) and (chip same power)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/04 15:05
13	BRS	L13	347	(power same min same max) and (cycles same plurality) and (chip same power)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/04 15:05
14	BRS	L14	62	(power same min same max) and (cycles same plurality) and (chip same power) and (summary same data)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/04 15:10
15	BRS	L15	1	(power same min same max) and (cycles same plurality) and (chip same power) and (summary adj data)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/04 15:06

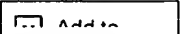

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	2	"6895561".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:11
17	BRS	L17	995	703/14.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:14
18	BRS	L18	487	703/14.ccls. and power	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:14
19	BRS	L19	17	703/14.ccls. and (power same min same max)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:14
20	BRS	L20	1	703/14.ccls. and (power same min same max same typ)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/04 15:14

Pro Quest Dissertations


Recent Searches

[Close window](#) | [Help](#)Add terms to your search using: 

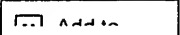

5. author(Kathirgamar Aingaran)
Database: Multiple databases...
Look for terms in: Citation and abstract
Publication type: All publication types

1 result [Set Up Alert](#) 

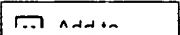

4. LPER({GAUTHIER, CLAUDE})
Database: Multiple databases...
Look for terms in: Citation and abstract
Publication type: All publication types

48 results [Set Up Alert](#) 

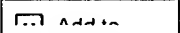

3. author(Claude R. Gauthier)
Database: Multiple databases...
Look for terms in: Citation and abstract
Publication type: All publication types

0 result [Set Up Alert](#) 

2. author(David J. Greenhill)
Database: Multiple databases...
Look for terms in: Citation and abstract
Publication type: All publication types

0 result [Set Up Alert](#) 

1. author(Mirian G. Blatt)
Database: Multiple databases...
Look for terms in: Citation and abstract
Publication type: All publication types

0 result [Set Up Alert](#) [Close window](#) | [Help](#)